CLAIMS

1. A memory system that couples to a host, said memory system comprising:

a plurality of storage elements, a first portion of said storage elements for providing low density storage, and a second portion of said storage elements for providing high density storage; and

a controller operatively connected to said storage elements, said controller operates to receive commands for data access from the host and to control reading and writing of data into said storage elements in accordance with the commands.

2. A memory system as recited in claim 1, wherein said storage elements are identical regardless of whether associated with the first portion or the second portion.

3. A memory system as recited in claim 1, wherein said storage elements are provided on a common substrate.

4. A memory system as recited in claim 1, wherein said memory system is provided within a single portable semiconductor memory product.

5. A memory system as recited in claim 1, wherein said storage elements configured for low density storage store one or two bits per cell, and wherein said storage elements configured for high density storage store four or more bits per cell.

6. A memory system as recited in claim 1, wherein said storage elements are non-volatile storage elements.

7. A memory system as recited in claim 1, wherein said storage elements are Flash type storage elements.

8. A memory system as recited in claim 1, wherein said storage elements configured for low density storage store one bit per cell, and wherein said storage elements configured for high density storage store two or more bits per cell.

9. A memory system as recited in claim 1, wherein said storage elements are Flash type storage elements.

10. A memory system as recited in claim 1, wherein said storage elements are EEPROM type storage elements.

11. A hybrid memory device having a single substrate, said hybrid memory device comprising:

a plurality of low density storage elements;

a plurality of high density storage elements; and

a controller operatively connected to said low density storage elements and said high density storage elements, said controller operates to control read, write and erasure of data into said low density storage elements and said high density storage elements.

12. A hybrid memory device as recited in claim 11, wherein said low density storage elements and said high density storage elements are memory cells.

13. A hybrid memory device as recited in claim 12, wherein said low density storage elements store one or two bits per cell, and wherein said high density storage elements store four or more bits per cell.

14. A hybrid memory device as recited in claim 12, wherein said low density storage elements store two bits per cell, and wherein said high density storage elements store four bits per cell.

15. A hybrid memory device as recited in claim 11, wherein said low density storage elements and said high density storage elements are Flash type storage elements.

16. A hybrid memory device as recited in claim 11, wherein said low density storage elements and said high density storage elements are EEPROM type storage elements.

17. A hybrid memory device as recited in claim 11, wherein said low density storage elements and said high density storage elements have a common device structure.

18. A hybrid memory device as recited in claim 17, wherein data stored to said low density storage elements can be read in substantially less time than it takes to read data from said high density storage elements.

19. A hybrid memory device as recited in claim 18, wherein the common device structure is a Flash device structure.

20. A hybrid memory device as recited in claim 18, wherein said hybrid memory device is a portable memory card having non-volatile memory, and

wherein said low density storage elements and said high density storage elements are non-volatile storage elements.

21. A portable memory card, comprising:

a data storage array, said data storage array including at least a first area of data storage having a first degree of robustness and a second area of data storage having a second degree of robustness; and

a controller operatively connected to said storage elements, said controller operating to control reading and writing to said data storage array.

22. A portable memory card as recited in claim 21, wherein said data storage array is provided on a single semiconductor chip.

23. A portable memory card as recited in claim 21, wherein the first area of data storage stores data with a first density, and wherein the second area of data storage stores data with a second density, the second density being at least twice that of the first density.

24. A portable memory card as recited in claim 21, wherein said controller is able to read data from the first area at substantially greater rates than is able to read data from the second area.

25. A portable memory card as recited in claim 21, wherein said controller stores data requiring greater robustness in the first area.

26. A portable memory card as recited in claim 21, wherein said portable memory card is a memory system on a chip.

27. A portable memory card, comprising:

a data storage array, said data storage array including at least a first area of data storage having a first density of data storage and a second area of data storage having a second density of data storage, the second density being at least twice that of the first density.

28. A portable memory card as recited in claim 27, wherein said data storage array includes data storage elements that have a common structure throughout said data storage array including the first area and the second area.

29. A portable memory card as recited in claim 27, wherein said data storage array is provided on a single semiconductor chip.

30. A portable memory card as recited in claim 27, wherein said portable memory card further comprises:

a controller operatively connected to said storage elements, said controller operates to control reading and writing to said data storage array

31. A portable memory card as recited in claim 30, wherein said controller is able to read data from the first area at substantially greater rates than is able to read data from the second area.

32. A portable memory card as recited in claim 31, wherein said controller stores data requiring greater read access speed in the first area.

33. A portable memory card as recited in claim 31, wherein said portable memory card is a memory system on a chip.

34. A method for rapidly forming an address translation table for a memory product having data storage elements arranged in logical blocks, each of the logical blocks including a plurality of data units, each of the data units having a header portion and a data portion, said method comprising:

(a) determining that the address translation table needs to be generated;

(b) reading the header portion of at least one of the data units within each of the logical blocks;

(c) determining physical addresses for each of the logical blocks from the corresponding header portion read; and

(d) forming the address translation table by saving the physical addresses in association with logical addresses for the logical blocks corresponding thereto.

34. A method as recited in claim 33, wherein the data storage elements are non-volatile.

35. A method as recited in claim 34, wherein the data storage elements operate in a low density storage mode and a high density storage mode.

36. A method as recited in claim 35, wherein the memory product further includes volatile storage, and wherein the address translation table is stored in the volatile storage.